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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,034	12/07/2001	Jozef D. Mitros	TI-32931	8951

23494 7590 05/27/2003

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EXAMINER

PHAM, LONG

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 05/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Advisory Action**

Application No.

10/020,034

Applicant(s)

MITROS ET AL.

Examiner

Long Pham

Art Unit

2814

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

**PERIOD FOR REPLY** [check either a) or b)]

- a) ☐ The period for reply expires \_\_\_ months from the mailing date of the final rejection.  
b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on \_\_\_\_\_. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.  
2. ☒ The proposed amendment(s) will not be entered because:  
(a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ they raise the issue of new matter (see Note below);  
(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See attached office action.

3. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
4. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attached office action.  
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: \_\_\_\_\_.

Claim(s) objected to: \_\_\_\_\_.

Claim(s) rejected: 1-30.

Claim(s) withdrawn from consideration: \_\_\_\_\_.

8. ☐ The proposed drawing correction filed on \_\_\_\_\_ is a) ☐ approved or b) ☐ disapproved by the Examiner.  
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_.  
10. ☐ Other: \_\_\_\_\_

Long Pham  
Primary Examiner  
Art Unit: 2814

## **DETAILED ACTION**

### ***Response to Amendment after final or Advisory Action***

#### ***Status of the amendment after final rejection***

New issues: The following proposed amendments raise new issues requiring further consideration and/or search:

Claim 8, line 4, claim 16, line 4, claim 22, lines 2-3, and claim 24, lines 4-5.  
Therefore, the amendment after final has not been entered.

#### ***Status of the pending claims after final rejection***

1. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242).
2. Claims 18, 19, 20, 21, 22, 23, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242).
3. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242).
4. Claims 28, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US '082) in view of Nakahara (US '242) (a

### ***Response to Arguments***

Applicant's arguments filed 11/18/02 have been fully considered but they are not persuasive.

In response to the applicants' arguments in the paragraphs on pages 4 and 5 of the amendment after final filed 11/18/02, it is submitted that the motivation for

performing the threshold voltage implantation of the first transistor and the source/drain formation implantation of the second transistor simultaneously as taught by Nakahar is to achieve high speed MOS devices as disclosed in col. 1, lines 54-60 of Nakahar patent. See the rejection. Alternatively, it is common knowledge that performing two ion implantations simultaneously would reduce processing steps.

In response to the applicants' arguments regarding the limitation of claim 2 in the paragraph on page 6, it is Lin et al teach implanting a portion of the first transistor to form source/drain regions. See the rejection.

In response to the applicants' arguments in the paragraph connecting pages 6 and 7, it is submitted that the motivation for performing the threshold voltage implantation of the third transistor and the source/drain or LDD formation implantation of the fourth transistor simultaneously as taught by Nakahar is to achieve high speed MOS devices as disclosed in col. 1, lines 54-60 of Nakahar patent. See the rejection. Alternatively, it is common knowledge that performing two ion implantations simultaneously would reduce processing steps.

In response to the applicants' arguments regarding the limitation of claim 4 in the paragraph on page 7, it is Lin et al teach implanting a portion of the third transistor to form source/drain regions. See the rejection.

In response to the applicants' arguments regarding the limitation of claims 18-30 in the paragraphs on pages 11-15, because the arguments are similar to the arguments regarding claims 1-17, the applicants are directed to the pending rejection and the Examiner's responses above.

***Conclusion***

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4082 for regular communications and 703-746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Long Pham

Primary Examiner

Art Unit 2814

L.P.

May 21, 2003